XLamp® LEDs Solder-Joint Reliability

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EXECUTIVE SUMMARY

Luminaire designers continue to push the operational requirements for LED lighting systems to higher output, higher temperature, longer lifetimes and more frequent on/off cycles. Cree LED has kept pace by introducing new LEDs with higher maximum drive currents, higher reliability on cycling, and better thermal performance. In applications such as Internet of Things (IoT) automated lighting systems, emergency vehicles, entertainment, and signal lighting, an LED may experience tens of thousands of on/off cycles. In these environments, the solder joint often becomes the first point of failure.

The reliability of the solder joint between the LED package and printed circuit board (PCB) is critical in ensuring the overall reliability of an LED lighting fixture. This application note describes best practices for creating reliable solder joints, the methods by which Cree LED tests solder-joint reliability, and methods for failure analysis of solder joints. Our thermal shock testing is a rigorous life test procedure that causes a significant acceleration in the evolution of failure mechanisms, thereby precipitating potential failures earlier than standard operational tests. Although thermal shock is instructive in identifying the most likely point of system failure under thermal stress, there is no direct correlation of thermal shock testing to real-world operating environments and these results should not be used as a predictive indicator of system lifetime or failure rates.

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INTRODUCTION

A typical LED package consists of various substrate materials, components, and encapsulants which vary with different manufacturers. The three primary material layers are:

1. The diode or “chip”, consisting of mostly silicon or sapphire with a thin layer of doped epitaxial GaN as the light-emitting layer. The diode has a thin AuSn layer for attaching to the LED substrate.
2. The LED substrate, typically AlN or Al_2O_3 in high-power components, or typically a plastic material like PCT in mid-power components. The LED substrate has copper metal traces terminated in gold or silver on the top for attaching the diode and on the bottom for attaching to the PCB.
3. The PCB, is typically a metal, like aluminum or copper, or a glass-fiber based FR-4 in less thermally demanding applications. The PCB also has thin copper traces for attaching the LED substrate and a thin dielectric layer to prevent shorting between electrical pathways.

The three joints between these layers and the final heat sink, whose integrity is critical to ensuring thermal transfer from the junction of the LED to the heat sink, are illustrated in Figure 1.

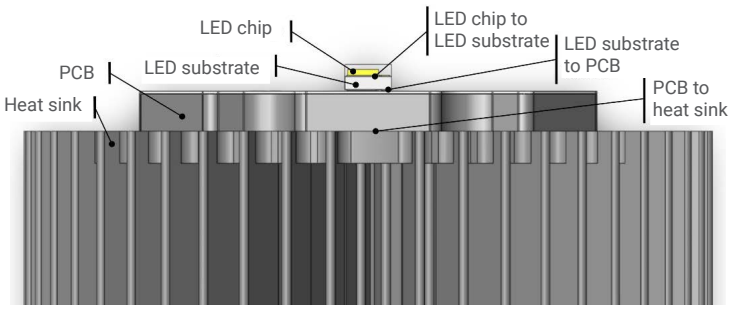

Figure 1: Points critical to ensuring thermal transfer from LED junction to heat sink

The LED manufacturer verifies the integrity of the LED chip to LED substrate joint. The PCB and luminaire assembly firm is responsible for verifying the integrity of the other two joints.

The integrity of the LED substrate to PCB solder joint is one of the key determinants of long-term lumen maintenance and reliability of LED products. Solder-joint reliability not only depends on the solder alloys, but also on the metallization of the LED package and PCB. In addition, the reflow profile also has a significant impact on lead-free solder-joint performance since it influences the wetting behavior and microstructure of the solder joint. A damaged or faulty solder joint can cause an open circuit failure that in turn can causes the complete electrical failure of the lamp or luminaire.

Thermal shock testing has a much more rapid ramp rate than thermal cycling, thus inflicting much more damage to solder joints. Thermal shock testing results can provide significant insight into the reliability of solder joints [3]. Cree LED’s ongoing research ensures the best possible reliability of solder joints for our high-power XLamp® LED packages.

The reliability of a solder joint is defined as the probability that the solder joint can perform the required function under specified operating conditions for a given time interval. Eutectic Sn63Pb37 solder (63% tin, 37% lead), which was historically the alloy of choice for soldering applications, has been replaced by lead-free solder alloys due to health and environmental concerns.

Solder-joint failures are a common failure mode observed in electronic packages [1]. The formation of a reliable solder joint depends on several factors such as the ability of the molten solder to rapidly and uniformly wet the surface finish and interact with it to form a consistent intermetallic layer at the interface [2]. The wetting behavior, interface chemistry, and metallurgical microstructure of the solder joint are determined predominantly by the reflow temperature. In addition, overall solder-joint reliability is determined by a combination of operating environment and system design. The operating environment determines the temperature extremes which the product must endure, frequency of on/off power cycling and the possibility of mechanical shocks or vibrational stresses [2].

For LED package to PCB reliability, the key characteristic to consider is the difference in thermal expansion coefficients between the LED package and the PCB material. Changes in operating conditions result in differential forces generated by expansion coefficient mismatch. These forces can be amplified by mechanisms such as LED substrate bending. For a larger LED package on a rigid PCB, the stress generated by expansion mismatch is highest within the solder joints furthest from the center of the LED package.

Figure 2 shows factors typically affecting LED solder-joint integrity. The factors shown in red are relevant to this study.

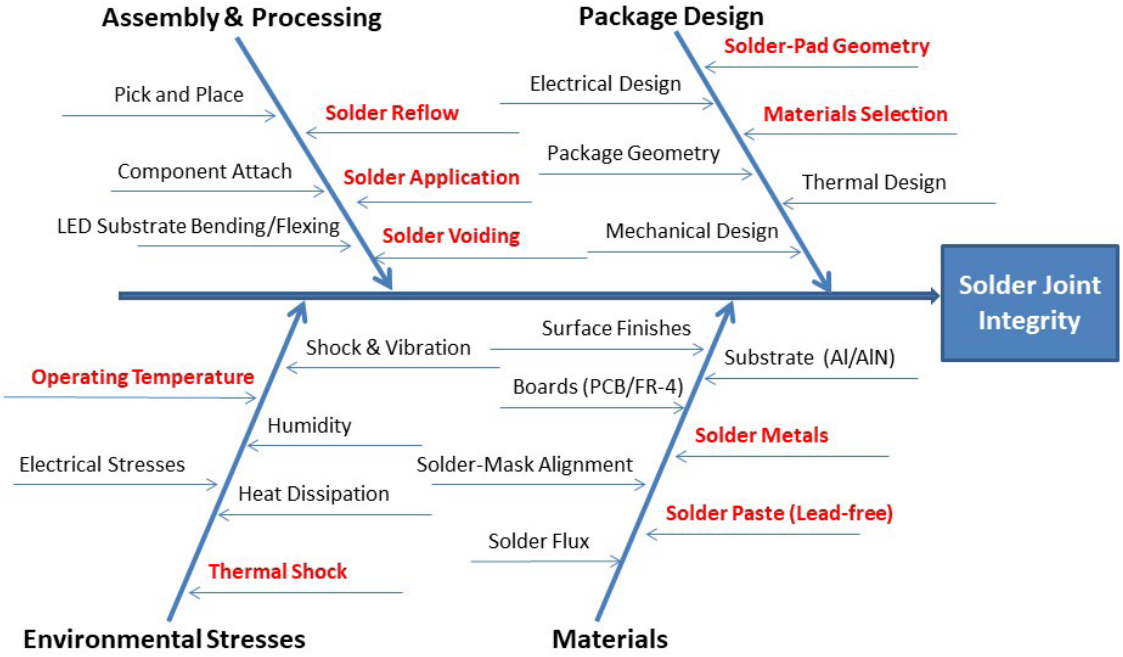

Figure 2: Factors typically affecting LED solder-joint integrity

Figure 3 illustrates the surface-mount technology (SMT) reflow process used with each LED package in this study.

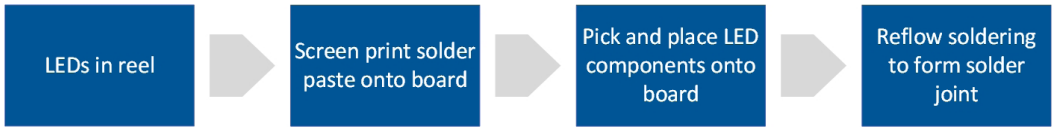

Figure 3: : Typical PCB assembly process

The stress per unit area experienced by thermal expansion of the LED joint is proportional to the size of the attach area. Larger components tend to have larger continuous bond pads and are more susceptible to cracking of the solder joint during thermal cycling. A general rule

of thumb is that smaller LEDs will have better thermal cycling reliability than larger LEDs, if all other thermal and materials considerations are constant. Package dimensions for Cree LED XLamp high-power LEDs are shown in Table 1.

Table 1: Component package dimensions for XLamp high-power components

XLamp Family Package	Length	Width
XQ-E, XQ-A, XD16	1.60 mm	1.60 mm
XE-G	2.05 mm	1.60 mm
XB-D	2.45 mm	2.45 mm
XP-G, XP-L, XP-P, XT-E, XHP35	3.45 mm	3.45 mm
XM-L®, XHP50	5.00 mm	5.00 mm
XHP70	7.00 mm	7.00 mm

REFLOW BEST PRACTICES USING LEAD-FREE SOLDERS

Lead-free solders differ from lead-based solders in their physical and metallurgical properties and process parameters such as melting point, surface tension, pre-heat and peak temperatures, soak and hold times and solder wetting behavior.

The melting temperature for Sn96.5 Ag3 Cu0.5 solder is between 217 °C and 219 °C, which is significantly higher than the eutectic Sn63 Pb37 solder, which has a melting point of 183 °C. This higher melting temperature requires requires reflow temperatures of 235-245 °C to achieve wetting and wicking. Lower peak temperature can be used only for boards with lower overall thermal masses or assemblies and do not have a large thermal mass differential across the board [4].

Lower peak temperature may also require extended soak time above the melting temperature. If the solderability of the component or board is poor, this lower temperature will also translate itself into poor wicking of solder and reduced spread [4]. Thus the formation of a reliable solder joint depends on the time and temperature profile of the solder reflow process, the ability of the molten solder to rapidly and uniformly wet the surface finish and interact with it to form a consistent layer of intermetallic at the interface [2].

All these factors can directly affect the formation and reliable performance of the solder joint. Cree LED's internal testing shows best results with a stencil opening design of approximately 65% solder coverage by bond area and a stencil thickness based on the largest dimension of the component.

- < 3 mm : 3 mil stencil
- 3.5 mm: 4 mil stencil
- 5.0 mm: 6 mil stencil
- 7.0 mm: 8 mil stencil

These guidelines may not be optimal for all systems. Do your own testing to validate your process for your unique requirements. Refer to the Soldering and Handling document in the Documents section of your LED's product page on the Cree LED website for our recommended reflow profile and temperature requirements.

X-RAY IMAGING

Commercially available X-ray imaging stations can be used to evaluate the solder attach to locate open contacts, shorts between the anode/cathode contacts and thermal pad, excess solder between the pads and solder voids.

X-ray Failure Criteria

Cree LED considers less than 30% solder voiding, i.e., less than 30% of the solderable area void of solder, to be ideal. Cree LED also considers solder voiding of greater than 50% to be a major contributing factor toward solder-joint failures. Other modes of failure are described in more detail below.

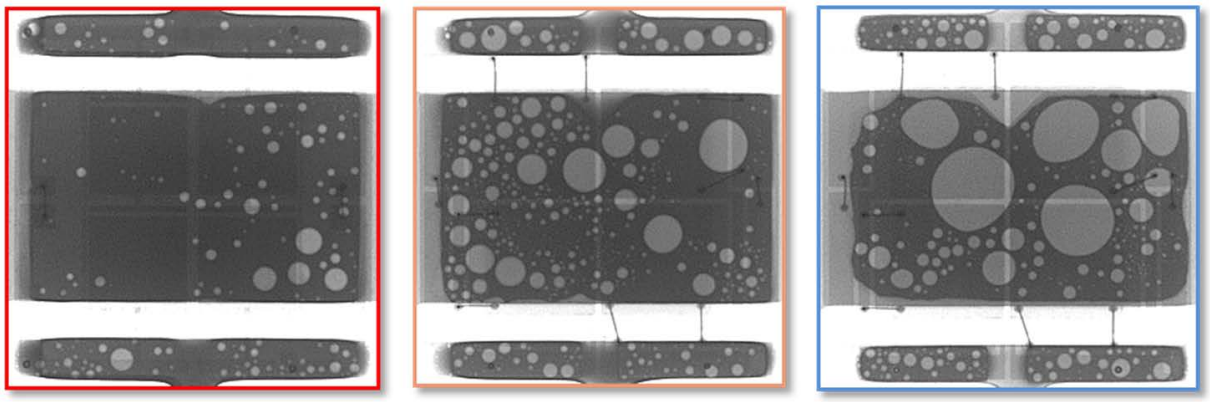

Figure 4: Showing voiding percentages (left to right) of approximately 10%, 30%, and 50%

Methods for Measuring Voiding in Solder Joints

A method called thresholding can be used to measure the percent voiding in an X-ray image of a solder joint. Various software programs can do this, or it can be manually programmed into image analysis tools and then automated for production. The process is as follows:

1. Find the total area, in pixels, of the bond pad attach area. This is typically the sum of three rectangles (anode, cathode, and thermal pad).
2. Adjust the image brightness and contrast until the void area is clearly white and the solder attach area is a dark grey or black.
3. Use the thresholding tool to set a grey value limit which falls in between the average grey values of voids and of solder. It is best to use the image's grey level histogram for this step, which should look bimodal. The tool will then change all lighter pixels to white and all darker pixels to black.
4. Count the number of white pixels (voids) within the bond pad rectangles and divide it by the total area of the bond pad rectangles. Check that the white pixels + black pixels is approximately equal to the pre-defined total attach area.

Failure Modes Identifiable by X-Ray Imaging

Not all failure modes can be seen with standard X-ray imaging. Solder-joint cracking typically propagates in the plane of the PCB, so there is no material density difference to observe from a bottom-up or top-down viewing perspective. This cracking is also difficult to observe from a side-view X-ray. The failure modes below can typically be identified in production to prevent field failures but may also be used to investigate field failures.

Excessive Voiding

The presence of excessive solder voids between the LED package and MCPCB is a reliability concern because voiding can compromise the thermal performance and electrical integrity, causing an increase in thermal resistance between the component and PCB.

Solder voiding is typically caused by:

1. Solder paste and solder paste flux formulation - Compared to tin-lead solders, lead-free solder alloys exhibit higher alloy surface tension which increases the propensity of solder voiding. The presence of aggressive flux chemistries in lead-free solders results in increased outgassing which leads to higher voiding.
2. PCB surface finish, e.g., OSP, immersion silver, gold/nickel, HASL - Due to the poor wetting of lead-free pastes compared to lead-based solders, PCB surface finish plays a critical role in void formation. Experiments on various PCB surface finishes suggest that immersion tin, immersion silver and lead-free HASL finishes are preferred for use with lead-free assembly [8].
3. Poor stencil design – Cree LED recommends a stencil design with many smaller openings with staggered alignment. In our testing, this design allows outgassing to escape through defined channels, reducing the average void diameter and total voiding volume. See the LED product data sheet for our recommended stencil design.
4. Process conditions – Deviations from the intended process conditions can cause voiding. These include insufficient reflow temperature or time, expired solder paste, and insufficient solder deposition.

The first two causes listed above are pre-defined by suppliers. The stencil design and process conditions are worth further discussion in the sections below.

Excessive Voiding Due to Stencil Shape and Window Arrangement

Cree LED has carried out extensive testing to determine the best possible solder paste stencil designs. Figure 5 shows three different stencil designs and the resulting voiding as shown by X-ray imaging. The more typical design on the left uses larger openings for the thermal pad, and completely covers the anode and cathodes. This design typically has adequate performance but has higher variability of voiding because it is hard to predict how gases escape from the joint.

Initial research suggested that using a higher number of smaller windows would help to control variability by designing the gas escape channels into the printed pattern. The middle column shows one of these designs. The thinner anode and cathode had very low voiding because of short gas escape paths. However, the “+” shaped channels in the middle of the thermal pad resulted in consistent trapping of small gas bubbles within the solder joint (as shown by the arrows).

The latest research iteration solved this problem by staggering the windows, as shown on the right column of Figure 5. This design predictably forces gas out in one direction in each channel, reducing total voiding even further.

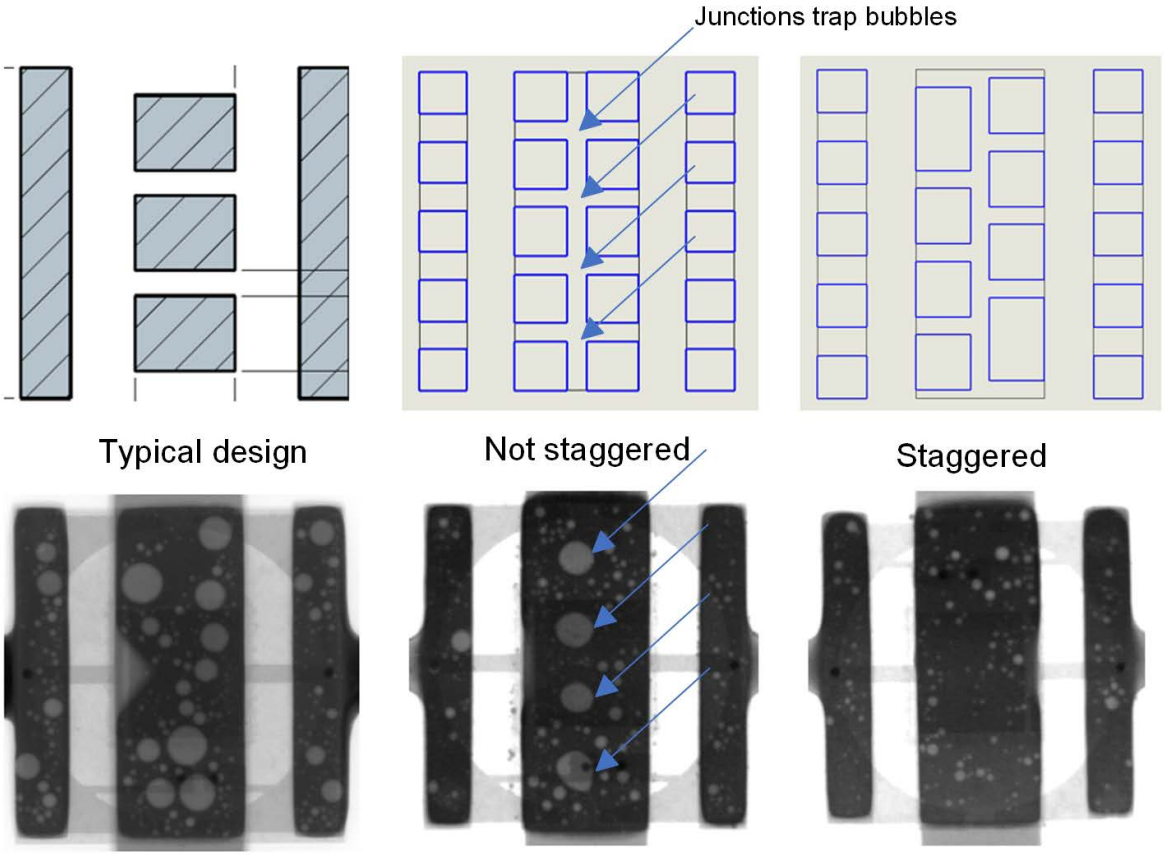

Figure 5: Improvements in voiding from updated stencil designs. Instead of using few large stencil windows, using many smaller windows tends to reduce large voids. Furthermore, staggering the windows prevents gas from being trapped at the channel junctions.

Controlled gas escape paths become more important as the size of the bond pads increases in larger components. Figure 6 shows an XLamp XHP50.3 LED recommended bond pad and stencil design. Here, the staggered channels printed on the thermal pads appear in 3 columns.

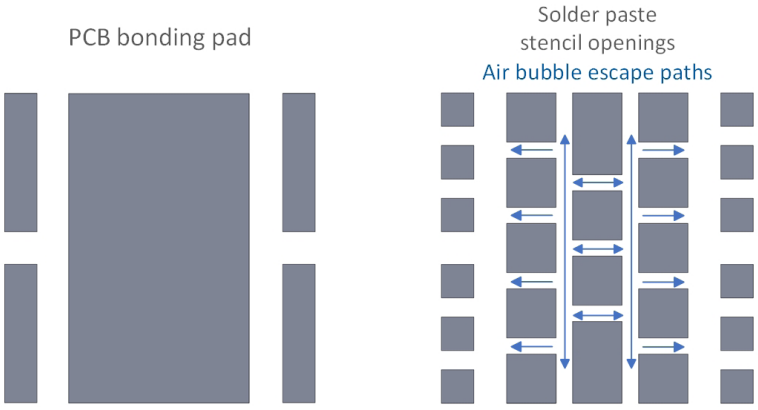

Figure 6: In larger footprints, providing channels for gases to escape is critical. The bond pad on the left has 65% of its area covered by the stencil pattern on the right.

Incomplete Solder Coverage Due to Insufficient Solder Paste Printing

A solder joint could have a perfect reflow but still be insufficiently formed due to sub-optimal volumes of solder paste deposited. This reduces the thermal contact area and can cause the LED to overheat at otherwise acceptable operating temperatures. This could be caused by:

1. Stencil designed with openings too small, or stencil thickness too thin.
2. Clogged or dirty stencil during deposition.
3. Dried out solder paste from incorrect storage or prolonged exposure to air.
4. Insufficient volume of paste applied to screen for printing.
5. Poor alignment or Z-height calibration of stencil to PCB, or squeegee force too low.

Figure 7 shows examples of incomplete solder coverage on the left and sufficient solder coverage with only small, dispersed voiding on the right. The component on the left will typically show degraded thermal performance and may fail prematurely due to overheating. Also note the contrast differences in these images. The solder paste on the right is darker grey because the solder is thicker and transmits fewer X-rays.

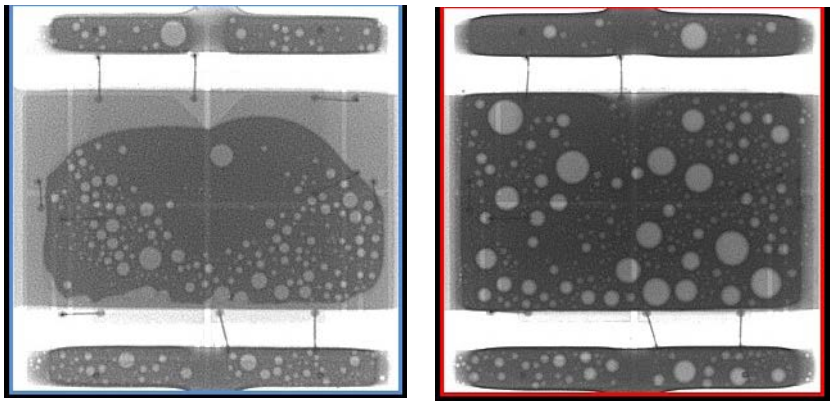

Figure 7: Showing the difference in appearance of partial (left) and complete (right) solder coverage.

Component Tilting, Misalignment, or Delamination Due to Insufficient Reflow Peak Temperature

Picking and placing LEDs onto PCBs is not always perfect and handling wet boards pre-reflow can cause shifting or twisting of components. However, if the correct temperature is achieved at reflow, the surface tension of the molten metal should cause the LED to snap back to the alignment of the PCB bonding pads. If full melting is not achieved, these placement and handling errors can cause partial LED attachment that could cause the PCB board to fail short or open.

Excessive Voiding Due to Insufficient Reflow Time or Temperature Conditions

The peak temperature of the reflow profile is not the only parameter that needs to be tightly controlled. The ramp rate, preheat time, and dwell times around the peak temperatures are all important factors in properly melting the solder and forming a metallurgical joint with optimal microstructure. The left image in Figure 8 shows large, uncontrolled voids resulting from an incorrect reflow profile that did not meet the manufacturer's recommended conditions (as shown in Table 2).

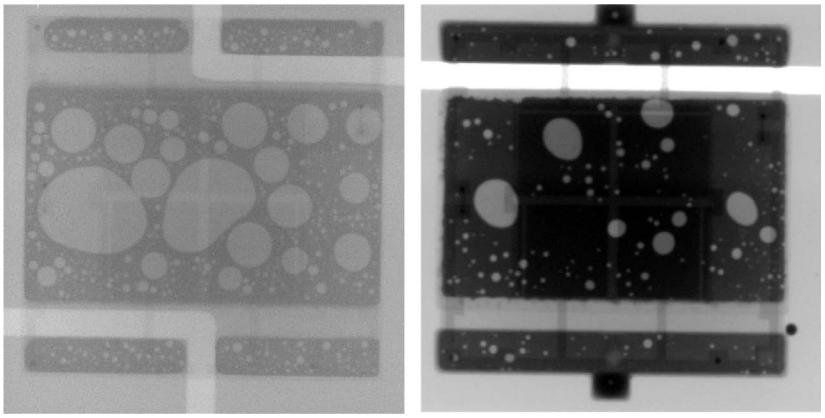

Figure 8: Excessive voiding due to insufficient reflow soak time and peak temperature (left) compared to optimized reflow profile (right).

Table 2: . Reflow profile parameters corresponding to the X-rays in Figure 8

Reflow profile parameters	Mfg. Data Sheet	Failed Profile	Correct Profile
Average Ramp-Up Rate (170 to Tp)	1.2 C/s	0.75 C/s	1.2 C/s
Preheat Time (120 to 170)	64-150 s	51 s	98 s
Time Maintained Above (217C)	40-90 s	39 s	72 s
Peak Temperature	235-245 C	231.5 C	244 C
Time Within 5C of Actual Peak	20-40 s	22 s	22 s
Ramp-Down Rate (Peak to 150C)	1-6 C/s	1.29 C/s	1.5 C/s
Time 25C to Peak Temperature	≤ 240 s	222 s	238 s

This failure can be caused not only by programming the temperature zones incorrectly, but also by measuring the real temperature of the PCB inaccurately. Cree LED uses a thermocouple soldered onto a PCB board of the intended shape, size, and materials specifications to test the reflow profile before each manufacturing run. The thermocouple has very long leads, allowing the board to pass through the oven while keeping the controller unit safely outside the front opening of the reflow oven.

The real temperature of the PCB nearly always deviates from the temperatures reported by the reflow oven control unit, so it is critical to manually measure the temperature before each production run.

THERMAL SHOCK TESTING

The most accelerated form of fatigue life testing is thermal shock, which is a type of temperature cycling with a high rate of temperature change [7]. The LEDs are soldered onto test boards which sit, not energized, in a temperature-controlled chamber that cycles between a high temperature (typically 125 °C), and a low temperature (typically -40 °C), over a specified duration of time. During thermal shock tests the solder joint experiences a temperature differential of 165 °C between the high and low temperature extremes.

During these rapid temperature changes, large thermal expansion differences develop between the various parts of the assembled board. This stress is caused not only by differences in expansion coefficients but also by temperature differences between the various parts. Large differential expansions cause large plastic deformations in the soldered joints, much larger than what can occur in real-life applications, where temperatures change slowly. The shock test therefore produces significant acceleration in the evolution of failure mechanisms thereby precipitating potential failures over a short period of time [7].

Thermal Shock Test Profile

The thermal shock testing used by Cree LED is based on JESD22 Method A104-E Condition G. In this testing, each solder joint is subjected to at least 200 cycles of thermal shock from -40 °C to 125 °C. Table 4 gives the thermal shock test profile.

Table 3: Thermal shock test profile

Test	Applicable Standards	Test Conditions & Failure Criteria
Thermal Shock	JESD22 Method A104-E Condition G	**Test Conditions:** • Temperature Range : -40 °C to 125 °C • Transfer Time : < 20 seconds • Cycles : 200 cycles **Failure Criteria [1]:** • LED no longer lights up after test

Note:

1. The entire test has failed if at least one LED from the sample set satisfies the listed failure criteria. If no LED satisfies the listed failure criteria, the test is successful.

Thermal Shock Induced Failure Modes

Thermal management is one of the most important factors that determine the long-term reliability of high-power LED packages. Most electronic failures are thermomechanically related, i.e., by the result of thermally induced stresses and strains or accelerated transport phenomena at higher temperatures. These thermomechanical failures are categorized as extrinsic failures because they often involve the electronic packaging [5].

In non-operating life tests like thermal shock, the sudden temperature changes cause concurrent degradation of the solder joint, resulting in intermetallic compound (IMC) growth and thermal fatigue damage. Thermal fatigue failures are one the most common failure modes associated with lead-free solder joints attributed to the differences in materials' coefficient of thermal expansion (CTE). These CTE differences are responsible for the development of stresses and mechanical strains at the material interfaces which results in fatigue-crack initiation and propagation in solder joints. CTE is a key material property that quantifies the degree to which a material will expand or contract as a result of a change in temperature [5].

Below we examine various solder-joint interface failures induced by accelerated thermal shock using scanning electron microscopy (SEM), energy dispersive X-ray (EDX) analysis and optical microscopy to evaluate the integrity of the joints and potential fatigue failure modes.

SOLDER-JOINT MICROSTRUCTURE

Cross sectional analysis was performed to analyze the behavior of solder joints after thermal shock tests and is shown in Figure 9. These cross-sections are created by mounting the failed component in epoxy, then polishing away material until the depth reveals the failure. We do not recommend using a saw to cross-section solder joints because the mechanical stress and vibration of cutting can alter the joint itself, masking the true failure.

The cross sections of the failed joints show that the fatigue fracture starts at the edge of the solder in most LED packages. Most of the fatigue cracks exist between tin and silver grains in the bulk of the solder trace and are propagated throughout the length of the solder in the direction of highest strain [6].

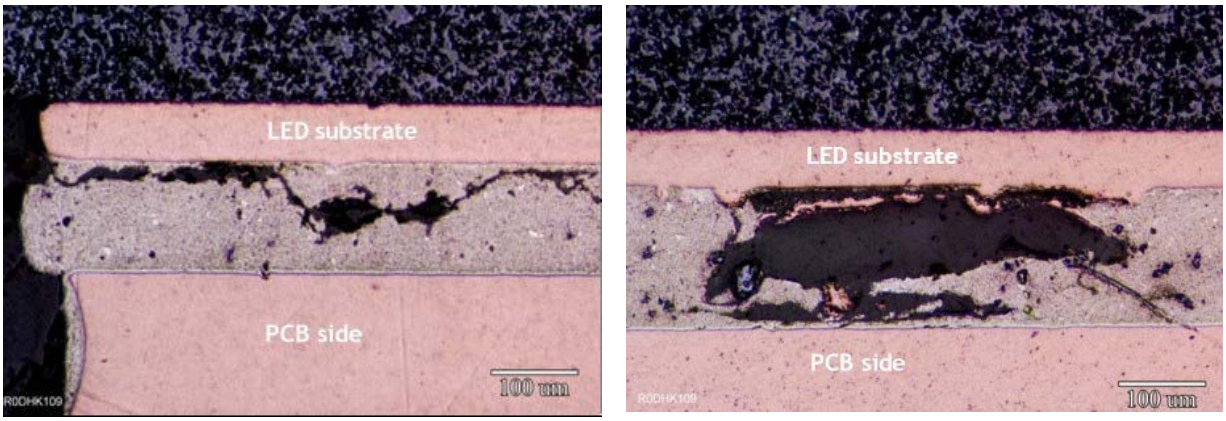

Figure 9: Cross-sections of failed solder joints imaged by an optical microscope, showing large voids and cracking along the plane of the joint

Cross-sectional studies showed the presence of solder cracks extending to the edges of the solder joint, which is the location of greatest stress concentration. These cracks occurred in the bulk of the solder extending from one edge of the solder joint to the other edge, decreasing the electrical performance and potentially causing mechanical failure of the solder joint. The cracks shown above are representative of solder-joint fatigue fracture typically associated with thermal-shock-induced stress which is attributed to the differences in the CTE between the mating/joining materials.

The size of the LED package has a significant impact on the development of cracks in the solder joints. Larger continuous attach areas in larger components cause more stress to build from CTE. Like gaps in a sidewalk, the gaps between the pads limit expansion and contraction stresses to a smaller area. Smaller components have smaller continuous pad areas and tend to be more resilient under thermal expansion stresses.

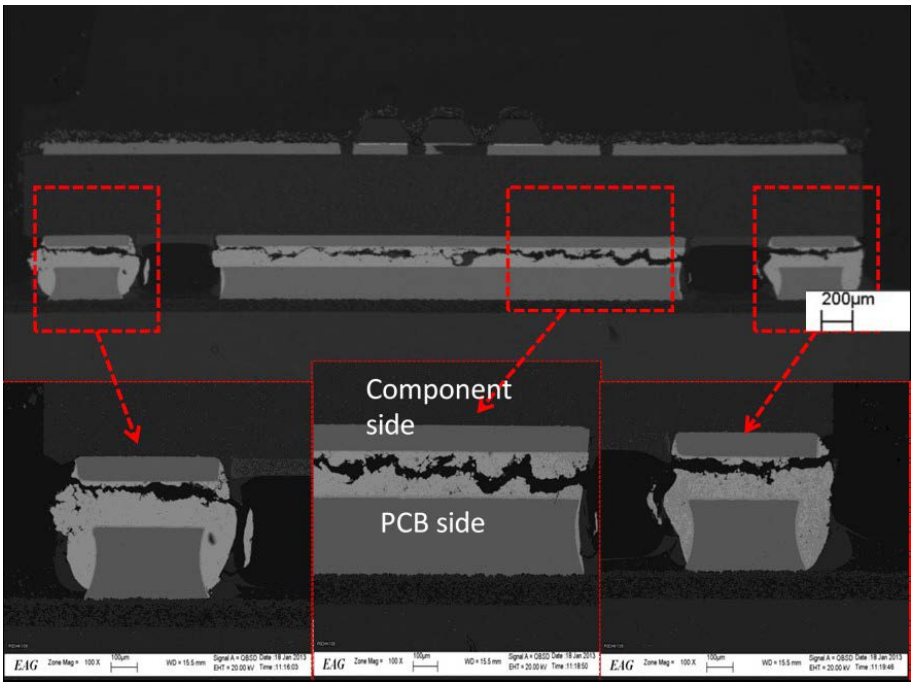

Figure 10: Cross-sections of failed solder joints imaged by a scanning electron microscope, showing cracking propagating along the plane of the joint

SUMMARY

This application note describes our methods for thermal shock testing and best practices for improving solder-joint reliability. These are the main takeaways:

- Total voiding area in production is a good predictor of solder-joint reliability.
- Larger components (5 mm and up) tend to fail more quickly than smaller components (4 mm and below) in thermal shock testing due to larger attach dimensions that build up more stress from thermal expansion.
- Premature solder-joint failures can be caused by many processing and design errors, including reflow temperature, solder paste handling, stencil design and surface finish.
- X-ray imaging of solder joints in production can identify processing errors and reduce field failures.
- Thermal shock testing does not directly predict LED operating lifetime due to differences in every unique application.

Lastly, to avoid premature solder-joint failures, always use the recommended solder-pad layout, solder paste and solder-reflow profile for XLamp LEDs as can be found in Cree LED's soldering and handling documents.

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